08/315934

CIRCUITS, SYSTEMS AND METHODS FOR IMPROVING PAGE ACCESSES AND BLOCK TRANSFERS IN A MEMORY SYSTEM

ABSTRACT OF THE DISCLOSURE

A memory 200 is provided which includes an array 201 of volatile memory cells 202. Addressing circuitry 205, 213 is included for providing access to selected ones of the memory cells 202. Master read/write circuitry 208 is included for reading and writing data into the selected memory cells 202. First slave circuitry 210, 211 is provided for storing data for exchange with the master read/write circuitry 208. Second slave circuitry 210/211 is also provided for storing data for exchange with the master read/write circuitry 208. Control circuitry 206, 214, 215 controls the exchanges of data between the master read/write circuitry 208 and the first and second slave circuitry 210, 211.

DA942290277/wpwin
090994tlm1
233:C3341-P07US-METH